

Code: 20ES1105

I B.Tech - I Semester – Regular Examinations - FEBRUARY - 2023

DIGITAL LOGIC DESIGN
(Common for AIML, DS)

Duration: 3 hours

Max. Marks: 70

Note: 1. This paper contains questions from 5 units of Syllabus. Each unit carries 14 marks and have an internal choice of Questions.

2. All parts of Question must be answered in one place.

BL – Blooms Level

CO – Course Outcome

			BL	CO	Max. Marks
UNIT-I					
1	a)	Explain BCD code and Excess-3 code with an example.	L2	CO1	7 M
	b)	Using 10's complement, subtract i) 72532 – 03250 ii) 03250 – 72532	L2	CO1	7 M
OR					
2	a)	Draw the symbol of Universal gates.	L2	CO1	7 M
	b)	Convert the following to Decimal and then to Octal (i) 4234 ₁₆ (ii) 10010011 ₂	L2	CO1	7 M
UNIT-II					
3	a)	Simplify the following Boolean function using K-Map. $F(w, x, y, z) = \sum m(0,1,2,3,5,9,12,14,15) + \sum d(4,8,11)$	L3	CO2	7 M
	b)	Construct the truth table of the function: $F = a'b'c' + ab'c + a'bc' + abc'$	L3	CO2	7 M

OR					
4	a)	Simplify the following Boolean expression using K-map. $F(W,X,Y,Z) = XZ+W'XY' +WXY+W'YZ +WY'Z$	L3	CO2	7 M
	b)	State and prove Demorgan's theorem.	L3	CO2	7 M
UNIT-III					
5	a)	Construct Binary Adder and explain the operation.	L3	CO3	7 M
	b)	Design 32:1 Mux using two 16:1 Muxs and one 2:1 Mux.	L3	CO3	7 M
OR					
6	a)	Implement the function $F = \sum m(0, 1, 2, 4, 5, 8, 11, 12, 15)$ using 8:1 Multiplexer.	L3	CO3	7 M
	b)	Design a Half Subtractor using logic gates.	L3	CO3	7 M
UNIT-IV					
7	a)	Convert the JK – Flip Flop into T - Flip Flop with truth table, characteristic table and excitation table.	L3	CO3	7 M
	b)	What is the drawback of SR- Flip Flop, design a Flip Flop which overcomes this drawback and explain with neat diagram.	L4	CO4	7 M
OR					
8	a)	Convert the SR- Flip Flop into the JK-Flip Flop. Draw and explain the logic diagram.	L3	CO3	7 M

	b)	Draw the circuit of SR- Flip Flop using gates and explain its operation.	L3	CO3	7 M
UNIT-V					
9	a)	Develop a 3-bit Ripple-Up counter.	L3	CO3	7 M
	b)	Design a 4-bit Synchronous counter with D Flip Flops and explain its working.	L3	CO3	7 M
OR					
10	a)	Draw the block diagram of an Asynchronous sequential circuit.	L3	CO3	7 M
	b)	Design a 4-bit shift register using D Flip Flops and explain its working.	L3	CO3	7 M